# A Study of Forward Error Correction Codes for SAS Channels

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*The SAS4 standard incorporates a Reed-Solomon (RS) forward error-correction (FEC) code. Other standards such as cache coherent interconnect for accelerators (CCIX) are also considering FEC for next-generation high-speed serial communication systems requiring low error rate over high loss channels. Both serial attached SCSI (SAS) and CCIX systems require link latency below 100ns, which severely constrains the choice of code and design of decoder. In this paper, we study error characteristics at the receiver for various SAS4 channels. We evaluate the performance of several choices of RS code and show how a frame-interleaved RS(30,26) code can achieve 1e-15 bit-error rate (BER) in the presence of burst errors. Furthermore, we studied the impact of 128/130 encoding scheme for a high insertion loss channel.*

The SAS 24G standard specifies an insertion loss of 30 dB [1]. In order to achieve the target bit error rate (BER) of 1e-15, forward error correcting (FEC) codes are considered. However, the SAS protocol relies on very low latency, which disqualifies most FEC codes currently deployed in networking applications.

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Over such a lossy channel it is very difficult to achieve the target BER of 1e-15 relying solely on pre-emphasis and decision feedback equalization [2][3]. Employing FEC is a natural solution to achieve the desired BER in SAS4 channels [4][5]. The aim is to achieve 1e-15 BER after FEC when the raw BER without FEC reaches 1e-6. At the same time the FEC must meet limits on acceptable power and latency increase.

Figure 1 shows the equalized pulse response of a typical long SAS4 channel, released by EMC to the SAS4 committee in August 2016. This channel has a large H1 value, which will lead to significant decision feedback equalization (DFE) error propagation. We use this EMC long channel in our initial SAS4 FEC study.

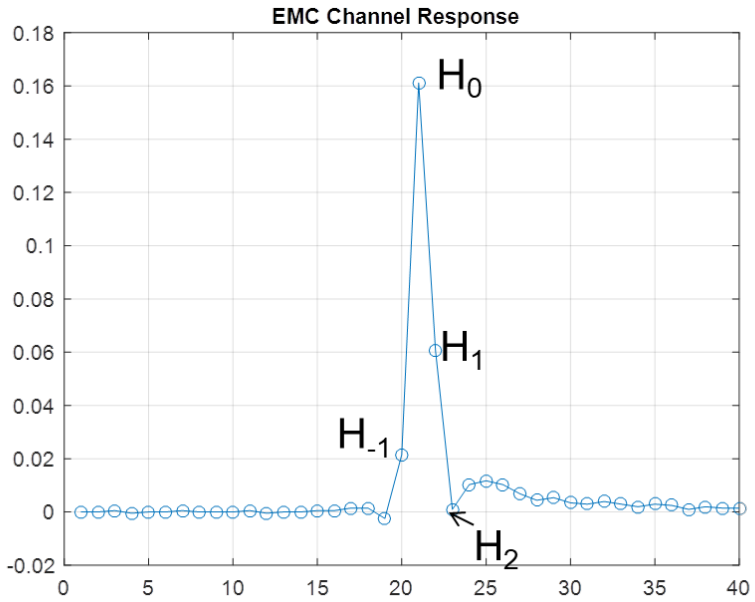


**Figure 1. Equalized channel response of EMC long channel**

Both encoding and decoding of a FEC will introduce latency. The latency associated with decoding is often significant [6]-[10]. The RS(30, 26) FEC selected by the SAS4 committee minimizes this latency impact because the data frame is short and because the error locations can be found directly, without the need for a Chien search.

The facts of the initial SAS4 RS FEC in our study:

- 128b/130b encoding is used instead of 8b/10b SAS3 encoding, added 01 or 10 to 128 data bits
- FEC is using RS (30, 26), T=2, 5-bit/symbol
- Data rate is 22.5 Gbit/s based on doubling SAS3 data rate of 12 Gbit/s with 8b/10b encoding

Figure 2 shows the FEC simulation results for EMC long channel with additive white Gaussian noise (AWGN) only. With raw BER 1e-6, we can only achieve 1e-10 after the single RS (30, 26) FEC code above. And we need around 1e-8 raw BER to achieve 1e-15 after FEC. The dash-line parts in the plot are extrapolated data.

To improve FEC performance in order to achieve 1e-15 after FEC at raw BER 1e-6, we studied two possible solutions:

(1) FEC with larger frame size and stronger error correction capability;
(2) Use frame interleave scheme to break long burst error.

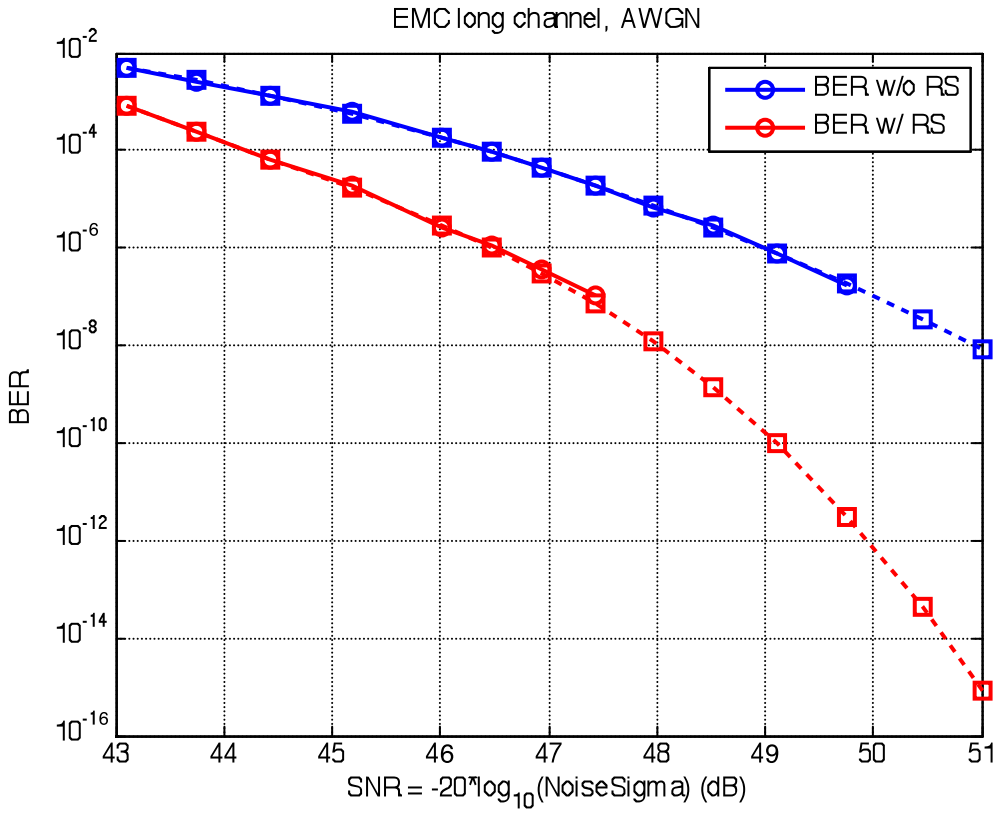


**Figure 2. FEC simulation results for EMC long channel with AWGN only.**

Figures 3 and 4 show two additional examples of the channel pulse response in a SAS storage system. These measurements were released by HPE to the SAS4 committee in August, 2016 and represent typical short and long reach applications. Please note that HP short channel has a very small H1 value, while HP long channel has a large H1 value. Figure 5 shows the frequency domain insertion loss characteristic for the three typical SAS4 channels studied in this paper.

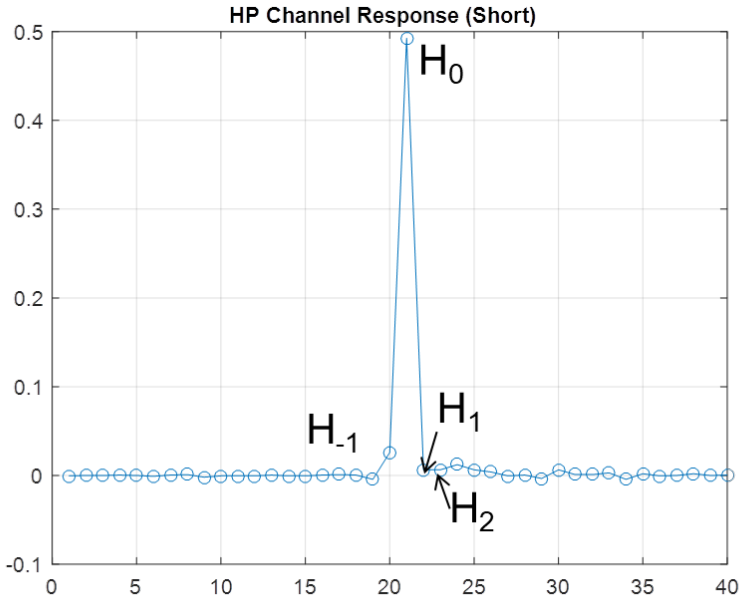


**Figure 3. Equalized channel response of HP short channel**

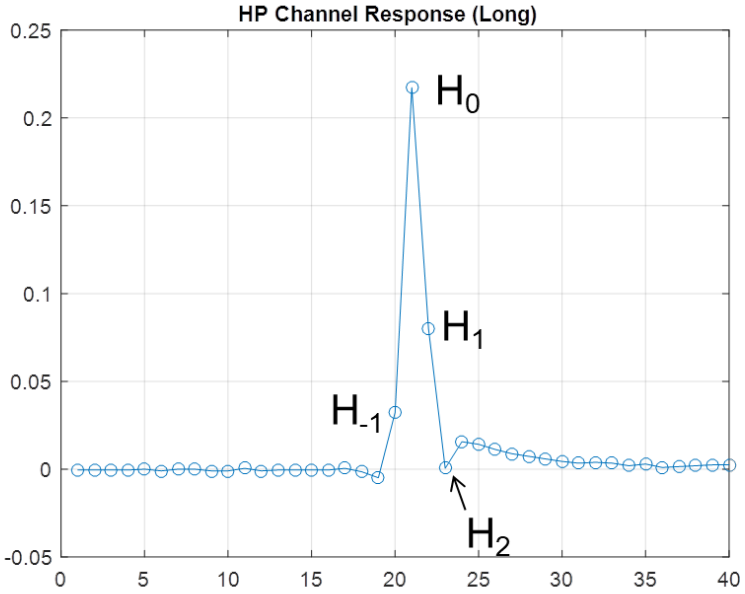


**Figure 4. Equalized channel response of HP long channel**

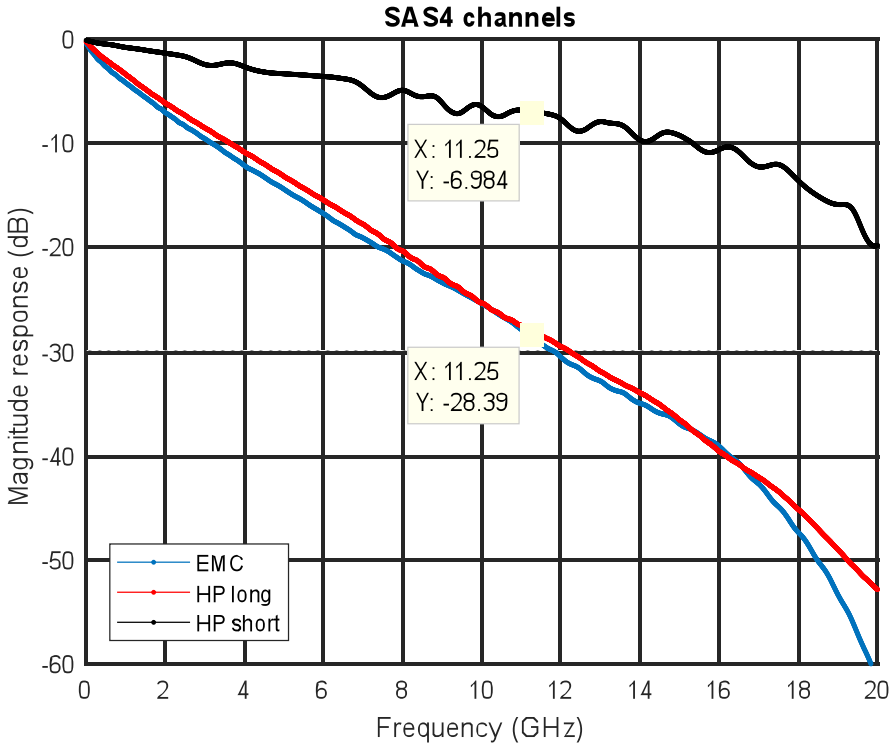


**Figure 5. Insertion loss for typical SAS4 channels.**

# Error Characteristics at Receiver Output

In this section, we examine the errors at the receiver output for data sent over the EMC long channel shown in Figure 1. In particular, we look at the distribution of the length of bursts of consecutive bits in error and the number of 5-bit symbols in error per FEC codeword.

**Burst length distribution**:

Figure 6 shows the burst length distributions at selected AWGN noise amplitudes. The longest burst observed was 10 consecutive bits in error, which could impact 3 consecutive 5-bit symbols. For the cases with higher signal-to-noise ratio (SNR), it is very unlikely that two or more short independent error events would affect the same frame and overcome the error correcting capability of the FEC. In these cases, there is still a significant likelihood that a single burst of 7 or more bits in error affecting three symbols could defeat the FEC.

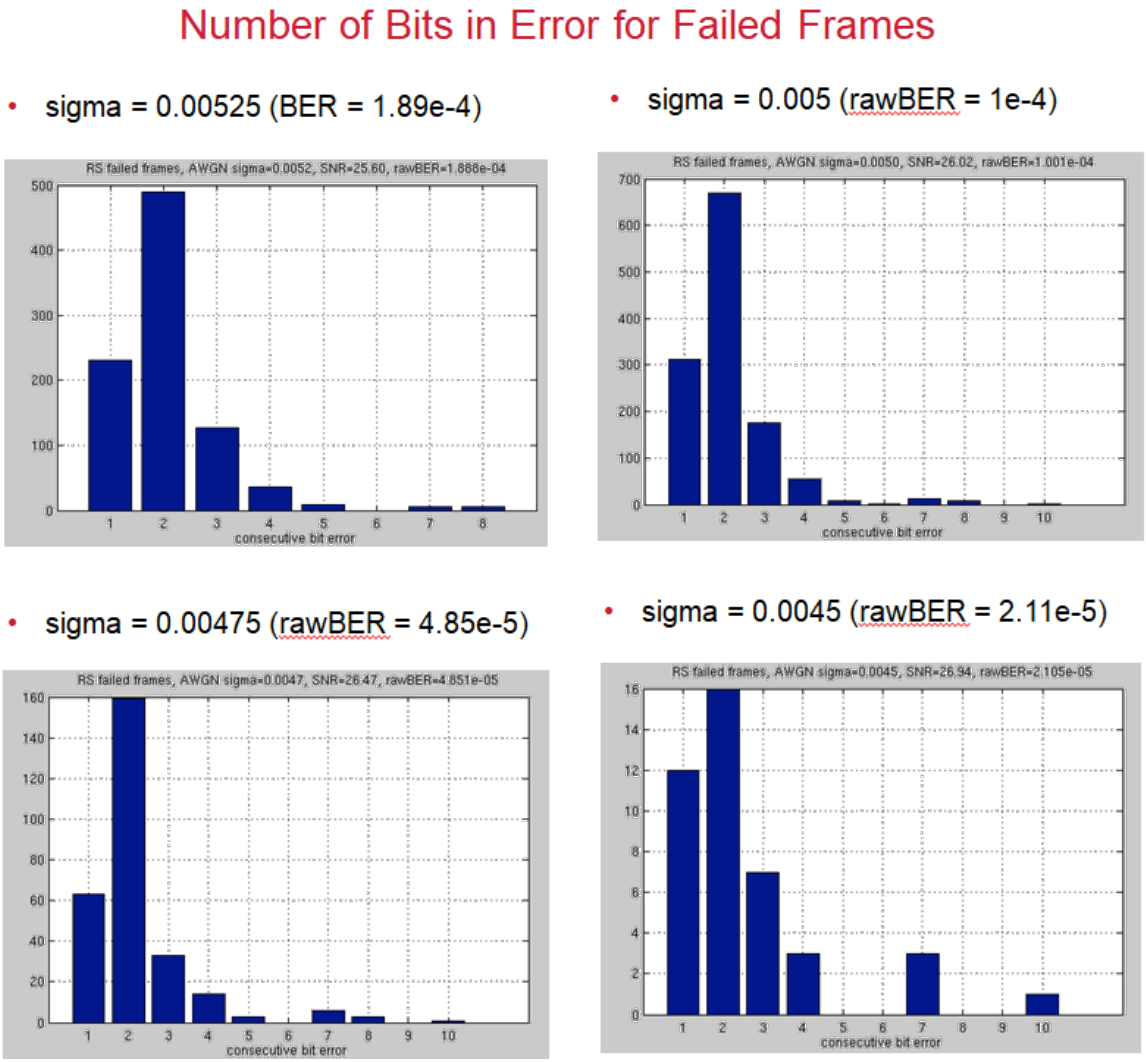


**Figure 6. Burst length distribution in EMC long channel.**

**Raw symbol error distribution**:

Figure 7 shows the distribution of symbols in error within the FEC frame. The symbol error distribution shows that the first and last symbols in each frame are more likely to be found in error than average. These locations are influenced by the header bits which take values of either 01 or 10. This observation can be explained by insertion loss related to the intrinsic Nyquist property of the 01 10 encoding overhead, and implied that using non-Nyquist patterns such as 128b/132b encoding (1100/0011) could be a better solution with slight increase on encoding overhead.

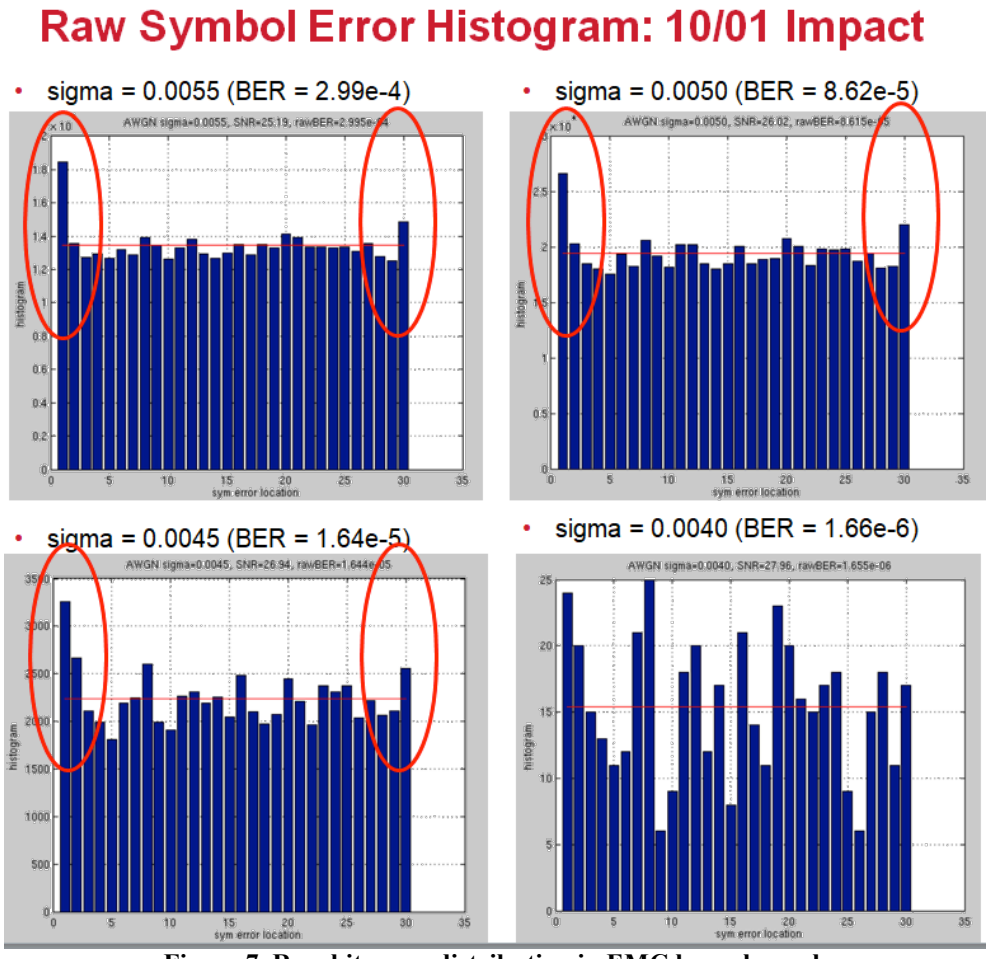


**Figure 7. Raw bit error distribution in EMC long channel.**

## Study on Two-Way Three-Way Frame Interleaving

The most likely failure mode for the SAS 24G FEC with high insertion loss channels is a single burst of 7 or more consecutive bits in error leading to three symbols in error. Interleaving code words offers a means of breaking up this error pattern without increasing the error correcting capability of the FEC, which would introduce additional overhead.

Figure 8 gives an example of interleaving two 150-bit frames so that consecutive symbols in error will impact different FEC code words. Similarly by extending the two-way interleaving to three FEC codewords any three consecutive symbol errors will be distributed into three different FEC codes. Interleaving in this way significantly reduces the impact of burst errors on FEC performance.

Without doubt, interleaving will introduce extra delay. However, with the short FEC code length we use, the interleaving delay could be controlled in an acceptable range.

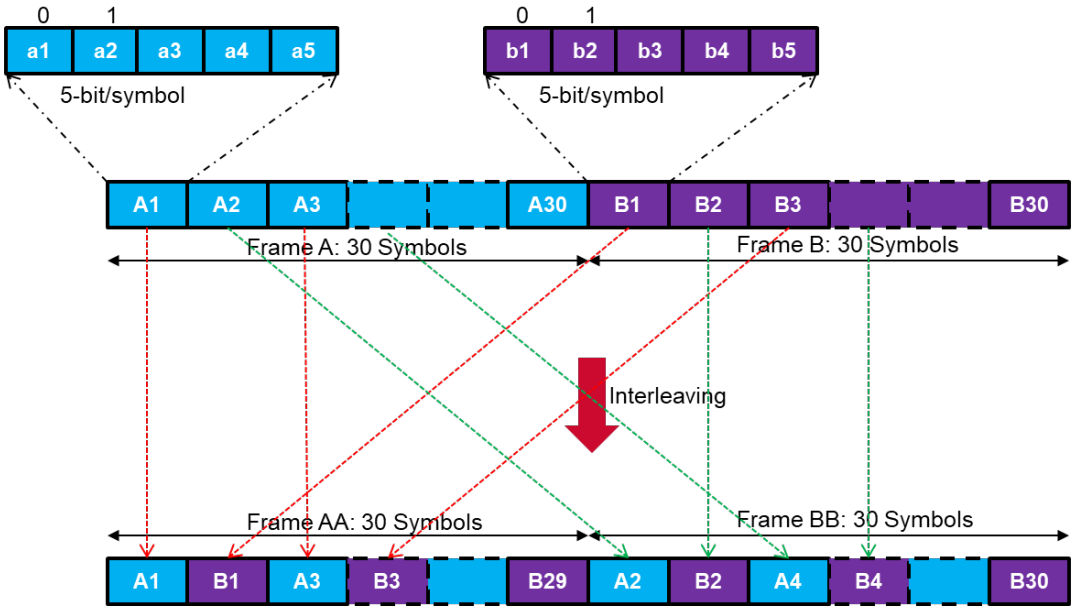


**Figure 8. An example of two-way interleaving.**

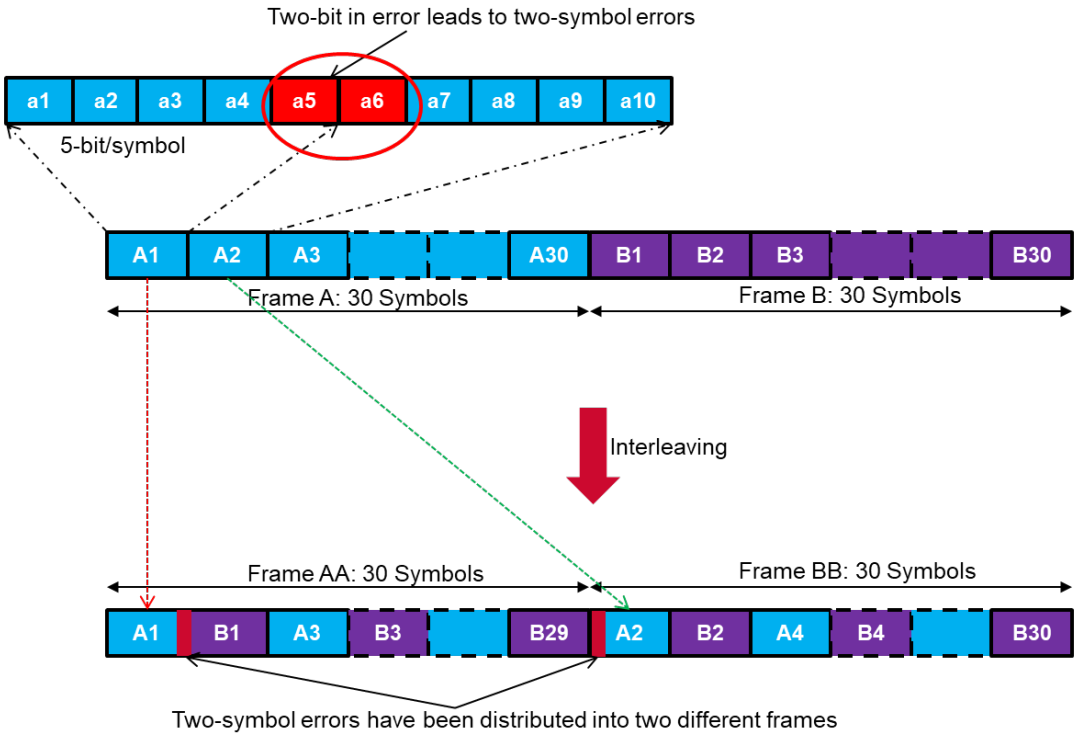


**Figure 9. Benefit of two-way interleaving.**

## Simulation Results:

Figure 10 shows the simulation results of two-way and three-way frame interleaving in HP short channel. For HP short channel, 1e-6 raw BER can achieve 3e-14 after FEC BER. HP short channel has a very small H1 value, which leads to less error propagation, i.e., less burst errors. Therefore, the benefits of frame interleaving are not significant in this circumstance. As shown in Figure 9, two-way and three-way interleaving brings very little performance gain for HP short channel, and this observation meets our expectation.

Figure 11 shows the simulation results of two-way and three-way frame interleaving in HP long channel. For HP long channel, 1e-6 raw BER can only achieve 2e-9 after FEC BER. HP long channel has a quite large H1 value, and it leads to more burst errors. As expected, two-way and three-way interleaving bring significant performance gain in our simulation results. By using two-way and three-way interleaving, 1e-6 raw BER can achieve 1e-14 region after FEC BER.

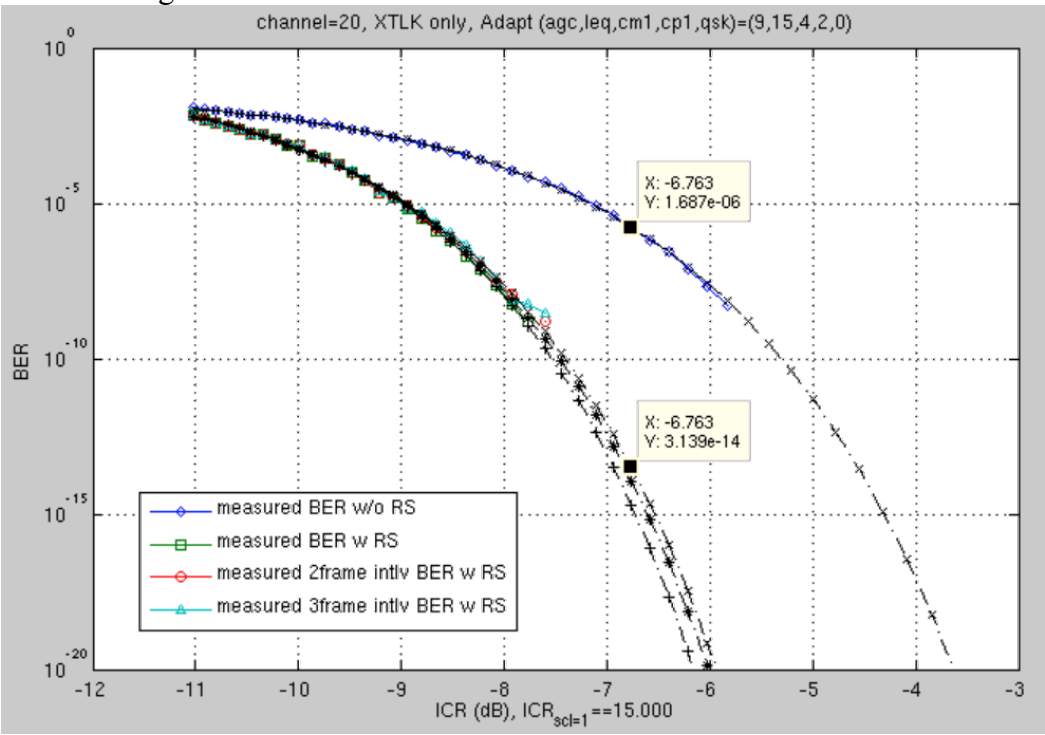


**Figure 10. Simulation results for interleave frame in HP short channel.**

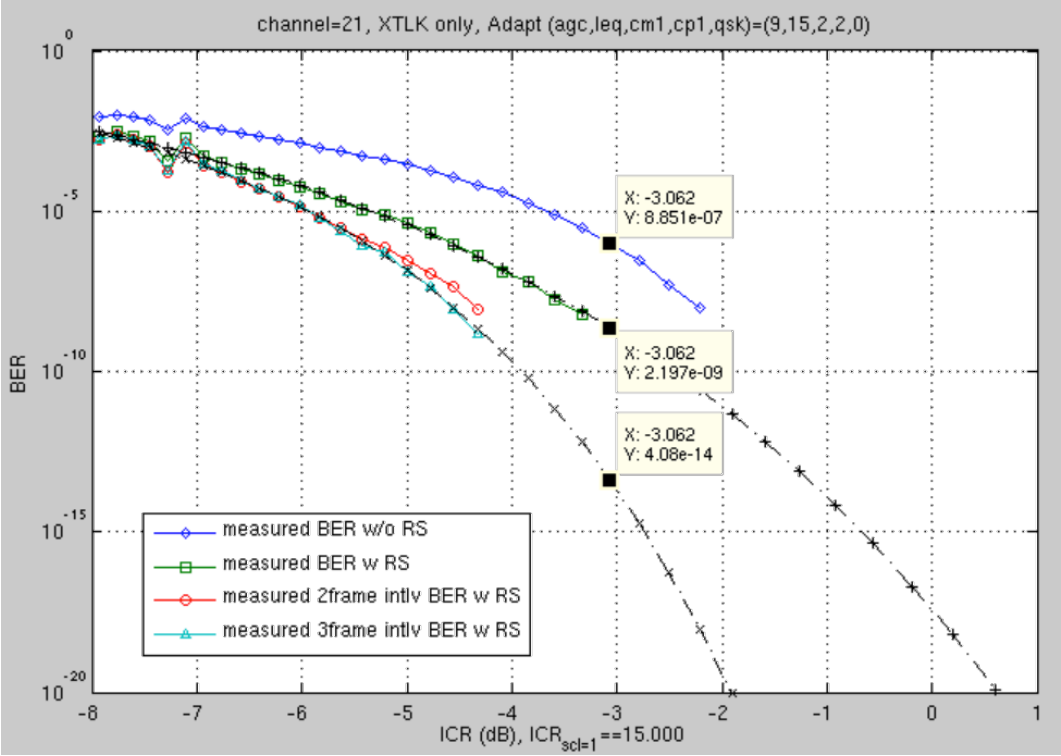


**Figure 11. Simulation results for interleave frame in HP long channel.**

# Study on RS Codes With Various Error Correcting Capability

To reduce introduced latency, we used a very short FEC code RS (30, 26). The disadvantage of the shorter FEC is that error correction is modest. The aim of our study is to find a good trade-off between code word length and error-correction capability of FEC for SAS4 channels.

Our study further compared the following three RS codes:

(1) Initial RS code with T=2, RS(30,26):
- 128/130 encoding (01,10)
- 5-bit per symbol, error correction capability T=2 symbols, code word length 150 bits
- code rate = 0.853, data rate 22.5GHz

(2) RS code with T=3, RS(50,44):
- 128/132 encoding (1100,0011)
- 6-bit per symbol, error correction capability T=3 symbols, code word length 300 bits
- code rate = 0.853, data rate 22.5GHz
- Need group two frames together to form an RS code word

(3) RS code with T=4, RS(52,44):

- 128/132 encoding (1100,0011)
- 6-bit per symbol, error correction capability T=4 symbols, code word length 312 bits
- code rate = 0.821, data rate 23.4GHz
- Need group two frames together to form an RS code word

As shown above, RS(30,26) and RS(50,44) have the same code rate, and the simulations use data rate 22.5GHz. However, RS(52,44) has a lower code rate, so its simulations use data rate 23.4GHz to compensate the code rate loss for a fair comparison.

**Simulation Conditions**:

For all the three RS codes above, we ran simulations with AWGN only and with AWGN/jitter/crosstalk combined noise for various SAS4 channels. All simulations have the following common conditions:

- Initial simulation settings are optimized for the specific channels;
- All adaptation loops are turned on;
- AC coupling 3dB corner is 0.3MHz;
- For simulations with AWGN/jitter/crosstalk (AWGN+Jit+Xtlk) combined noise, the static/random jitter noise and crosstalk noise are with fixed amount, and only AWGN sigma is changing.

**Simulation Results**:

We have shown in Figure 2 that RS(30,26) code is not strong enough to handle EMC long channel. RS codes with better error-correction capability are needed for SAS4 channel in order to meet raw BER = 1e-6 to after FEC BER = 1e-15.

Figure 12 and Figure 13 show the simulation results of RS(50,44) in EMC long channel with different noise properties. Figure 11 is for EMC long channel with AWGN only, where 1e-6 raw BER can achieve 5e-12 after FEC BER. Figure 12 is for EMC long channel with AWGN+Jit+Xtlk combined noise, where 1e-6 raw BER can achieve 1e-11 after FEC BER.

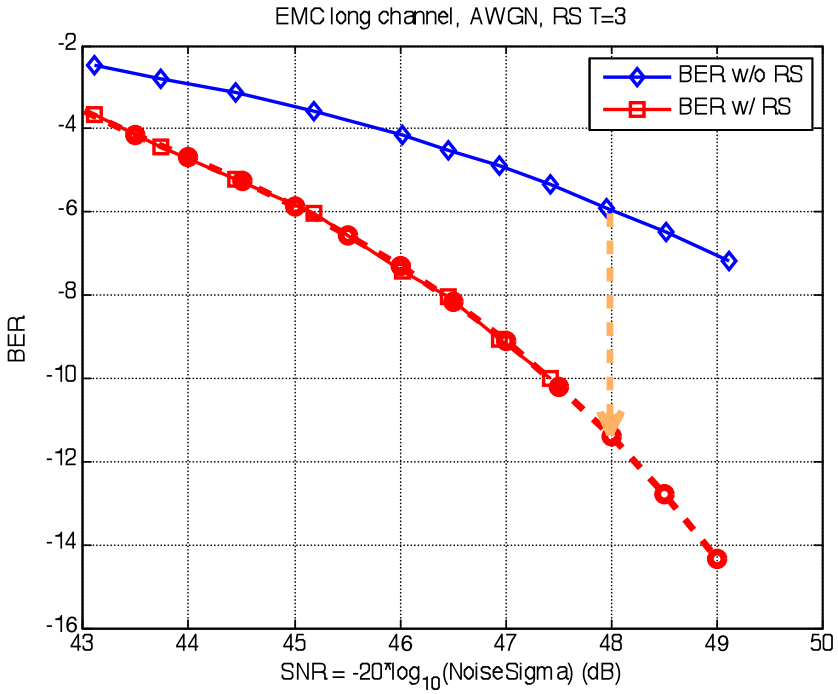


**Figure 12. Simulation results for RS (50,44) code with T=3 in EMC long channel: AWGN only, 22.5GHz.**

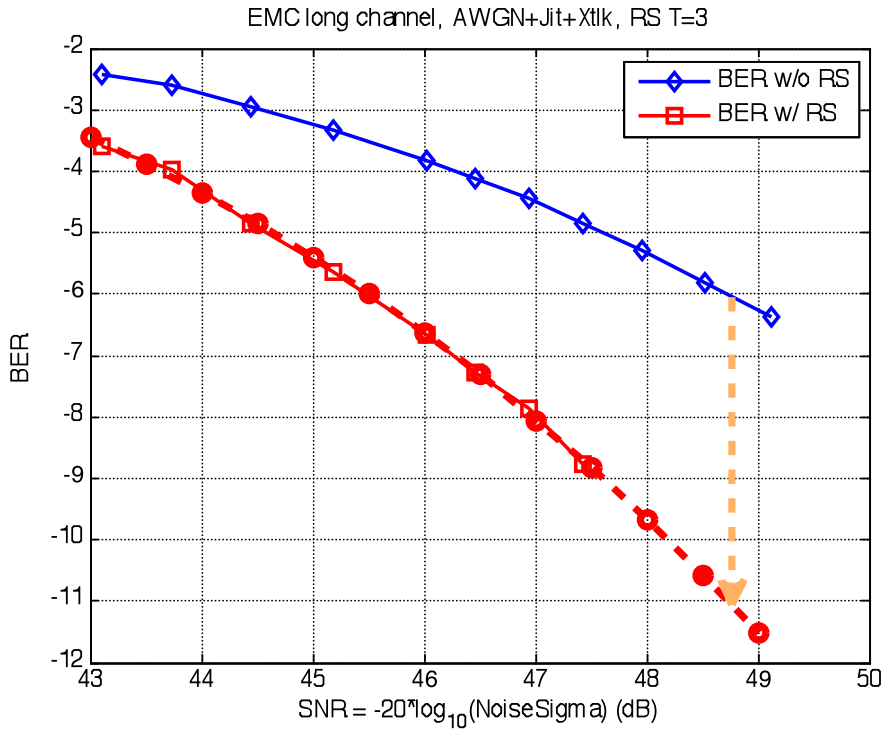


**Figure 13. Simulation results for RS (50, 44) code with T=3 in EMC long channel: AWGN+Jit+Xtlk, 22.5GHz.**

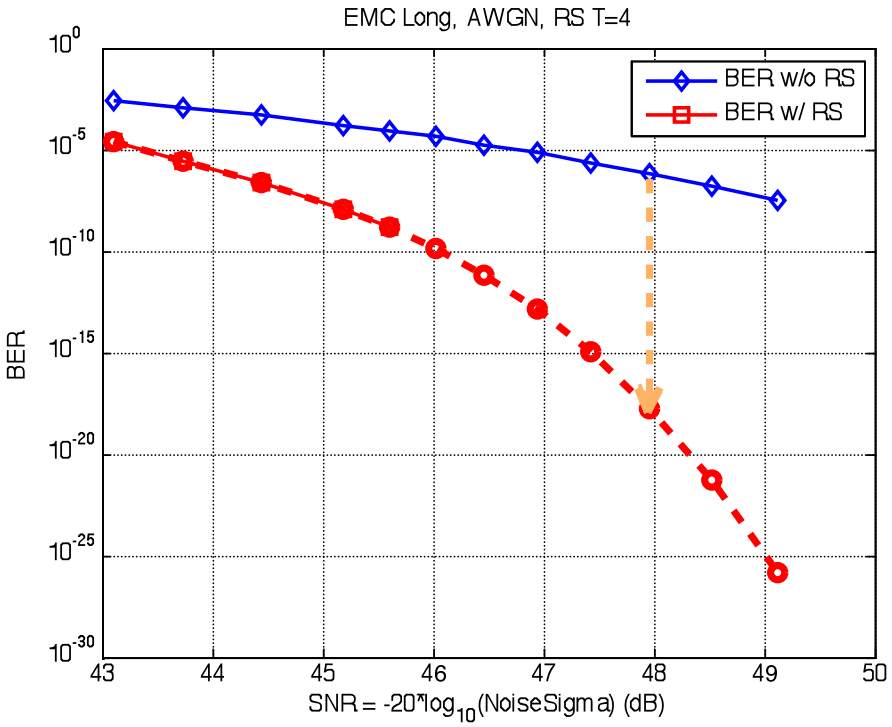


**Figure 14. Simulation results for RS (52,44) code with T=4 in EMC long channel: AWGN only, 23.4GHZ.**

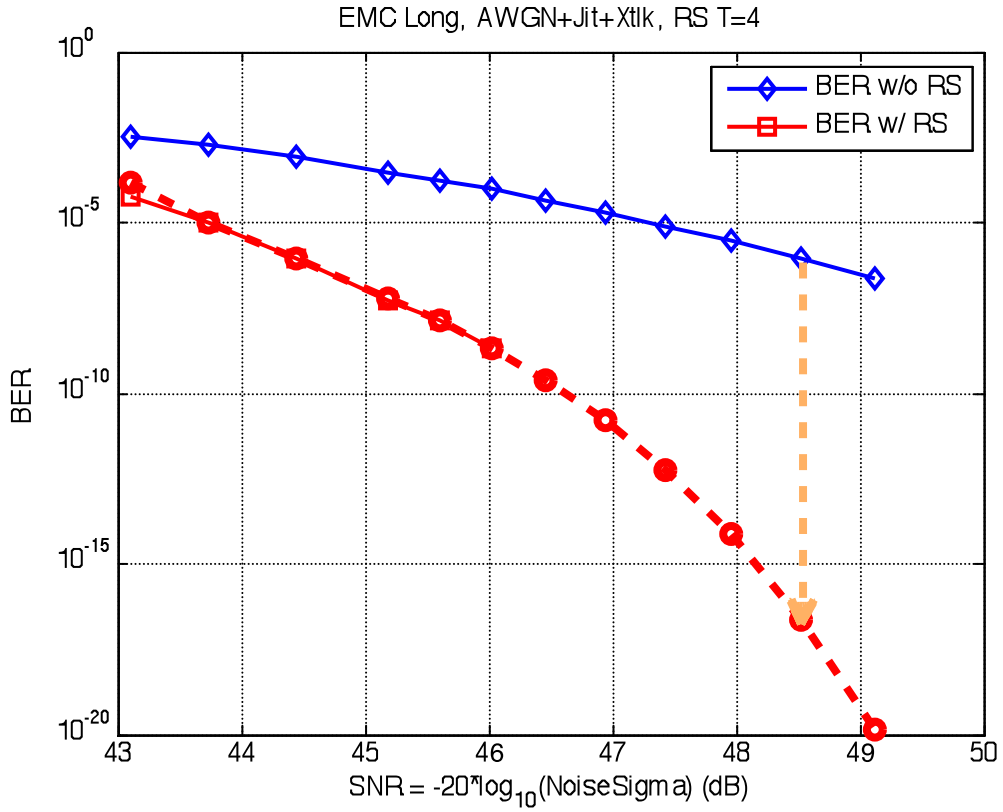

**Figure 15. Simulation results for RS (52,44) code with T=4 in EMC long channel: AWGN+Jit+Xtlk, 23.4GHz.**

Figure 14 and Figure 15 show the simulation results of RS(52,44) in EMC long channel with different noise properties. Figure 13 is for EMC long channel with AWGN only, where 1e-6 raw BER can achieve 5e-18 after FEC BER. Figure 14 is for EMC long channel with AWGN+Jit+Xtlk combined noise, where 1e-6 raw BER can achieve 5e-17 after FEC BER.

Figure 16 and Figure 17 show the simulation results of RS(52,44) in HP long channel with different noise properties. Figure 15 is for HP long channel with AWGN only, where 1e-6 raw BER can achieve 5e-14 after FEC BER. Figure 16 is for HP long channel with AWGN+Jit+Xtlk combined noise, where 1e-6 raw BER can achieve 4e-15 after FEC BER.

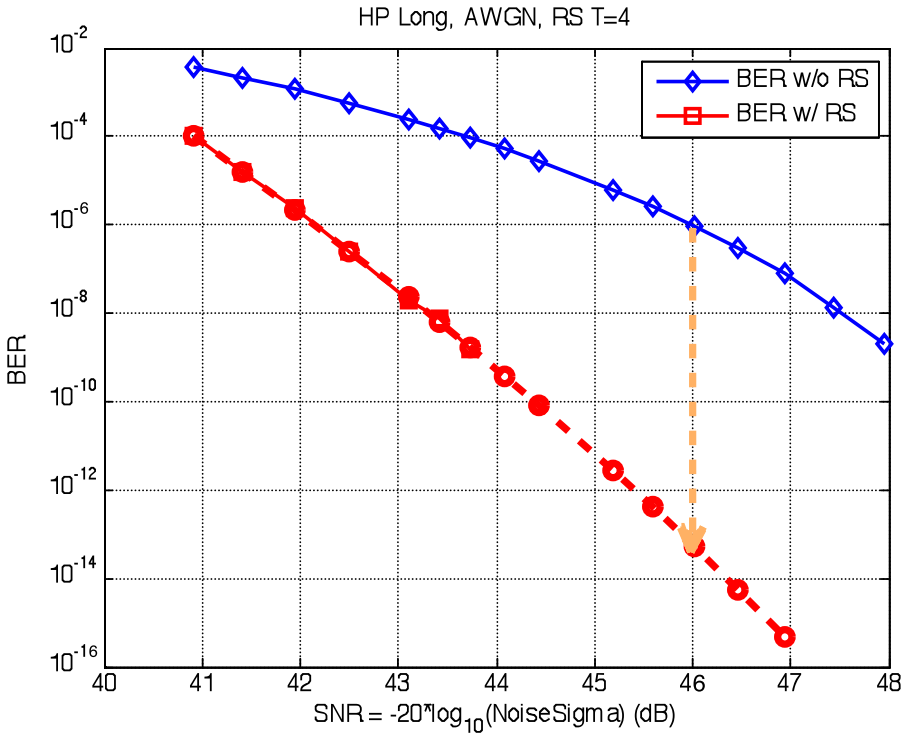


**Figure 16. Simulation results for RS (52,44) code with T=4 in HP long channel: AWGN only, 23.4GHZ.**

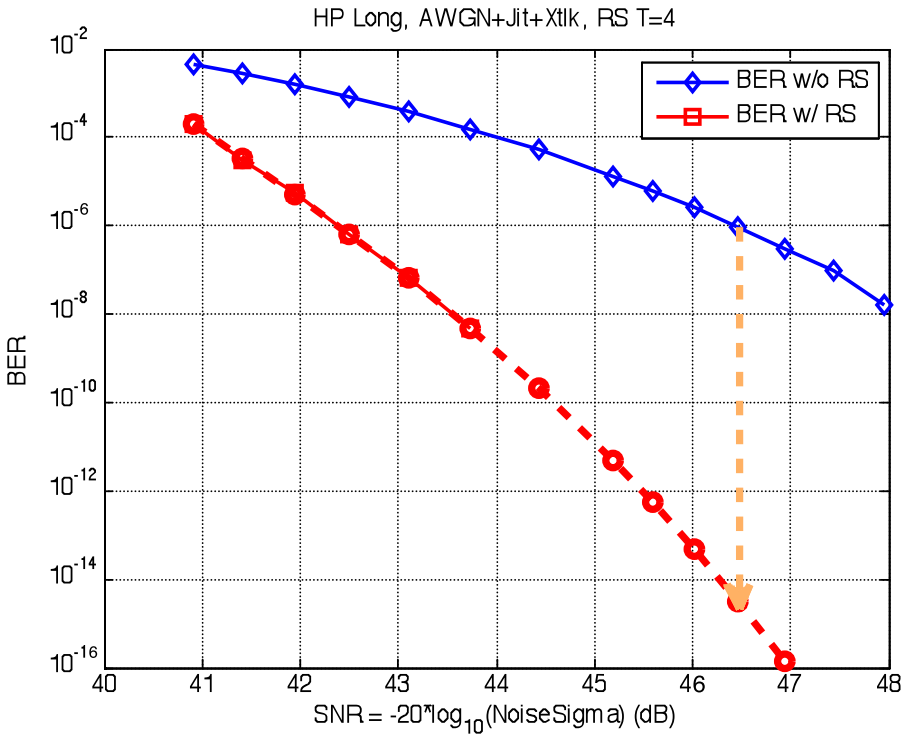


**Figure 17. Simulation results for RS (52,44) code with T=4 in HP long channel: AWGN+Jit+Xtlk, 23.4GHz.**

Figure 18 and Figure 19 show the simulation results of RS(52,44) in HP short channel with different noise properties. Figure 17 is for HP short channel with AWGN only, where 1e-6 raw BER can achieve 1e-20 after FEC BER. Figure 18 is for HP short channel with AWGN+Jit+Xtlk combined noise, where 1e-6 raw BER can achieve 4e-20 after FEC BER.

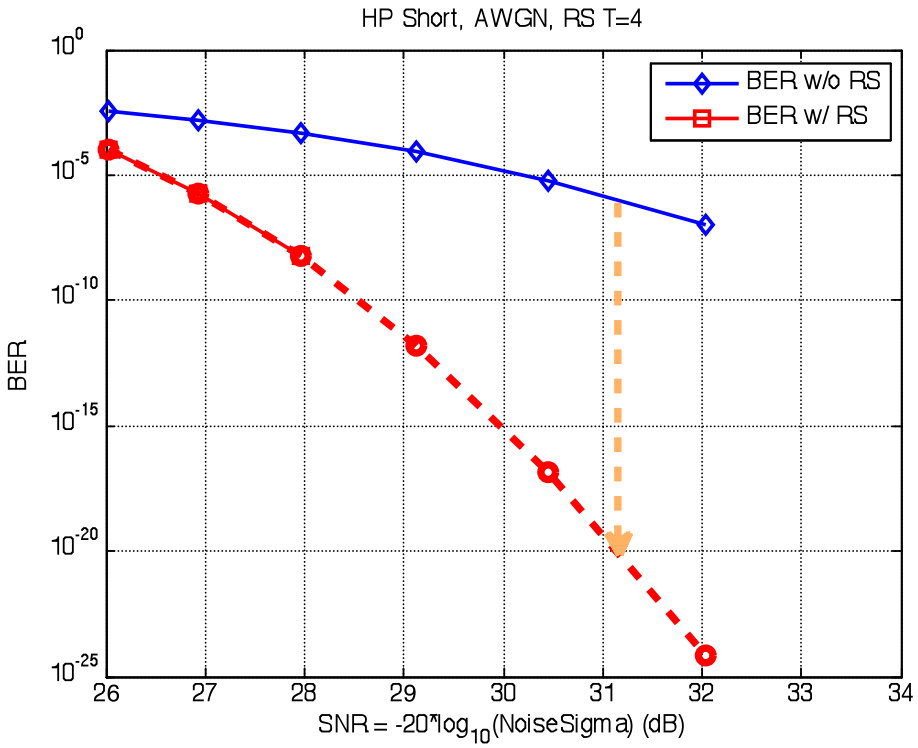


**Figure 18. Simulation results for RS (52,44) code with T=4 in HP short channel: AWGN only, 23.4GHZ.**

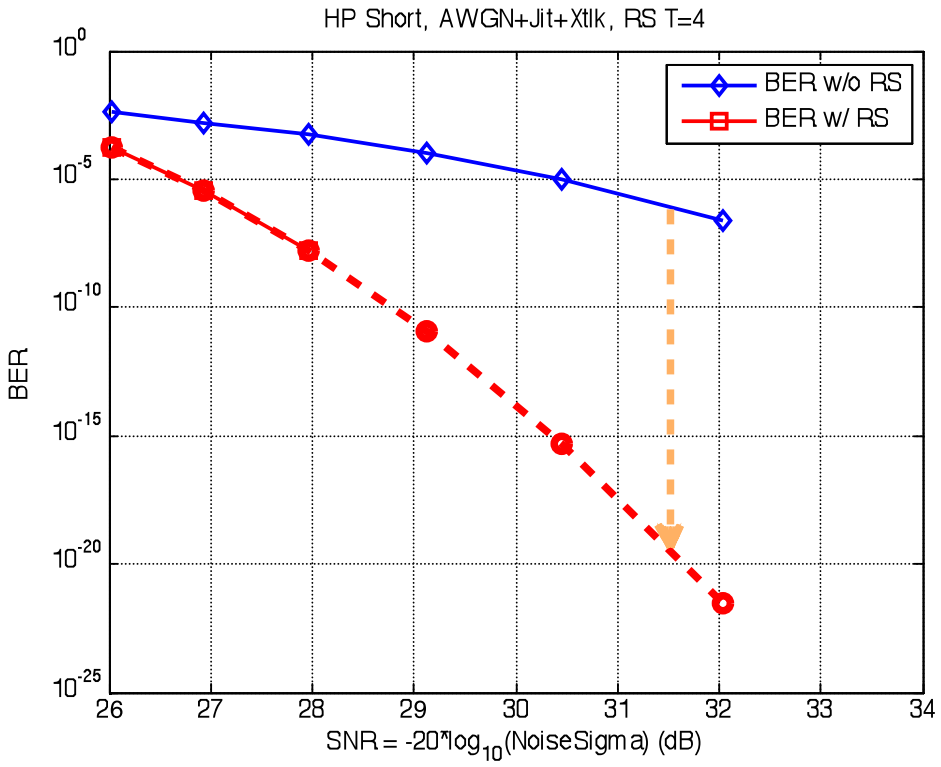

**Figure 19. Simulation results for RS (52,44) code with T=4 in HP short channel: AWGN+Jit+Xtlk, 23.4GHz.**

# Conclusions

The study in this paper shows that a strong FEC code such as RS(52,44) with error correction capability T=4 can be used in order to achieve after FEC BER around 1e-15 with raw BER = 1e-6. If strong FEC codes are not an option because of implementation complexity, then an interleaving scheme can be used to serve the purpose. With the channels we have simulated, it looks like three-way interleaving performance is very close to two-way interleaving of SAS4 FEC codes.

As data rates go higher with insertion loss becoming bigger, we strongly believe that current 128b/130b encoding is not a good option as the two-bit 01/10 overhead suffers due to its Nyquist pattern property.

*An earlier version of this paper was a DesignCon 2018 Best Paper Award Winner.*

# Author(s) Biography

**Haitao (Tony) Xia** is Distinguished Engineer of R&D at Broadcom Ltd, leading the research and development of advanced read channel and Serdes architectures for data storage systems. Dr. Xia served as Chairman of IEEE Data Storage Technical Committee and President of Chinese American Information Storage Society (CAISS) in the past. Before his work at Broadcom/Avago/LSI, Dr. Xia worked at Silicon Valley start-up, Linked-A-Media Devices, on signal processing and coding in the area of magnetic recording channels and non-volatile memories. Dr. Xia has published more than 20 articles in peer-reviewed journals/conferences, and has more than 120 US patent granted to his name. Dr. Xia is an IEEE Senior Member.

**Haotian Zhang** is a Principal Engineer of R&D at Broadcom Ltd in Longmont, CO., working on the research and development of advanced read channel and Serdes architectures for data storage systems. He holds PhD (2005) degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, and MS (2000) and BS (1997) degrees in electrical engineering from Tsinghua University, Beijing, China. Before his work at Broadcom/Avago/LSI, Dr. Zhang worked at Marvell and Maxtor on signal processing in the area of magnetic recording channels and optical channels..

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**Bruce Wilson** is Director of Architecture at Broadcom's Data Controller Division and worked to advance signal processing and electronics for Data Storage for more than 20 years. Bruce received his Doctorate at Stanford University and has worked at IBM, HGST, LSI and Broadcom.

**Jun Yao** is currently at Etopus, a Silicon Valley startup to make fast connections. Dr. Yao worked at Broadcom as Senior Engineer and Postdoctoral Researcher at Carnegie Mellon
University, PA. He obtained his PhD degree (2013) in electrical and electronic engineering from Nanyang Technological University, Singapore, and bachelor degree (2008) from Harbin Institute of Technology, China. His research interests include signal processing, equalization, phase-locked loop, detection and decoding algorithms for the hard disk drive (HDD) read channel and high-speed Serializer/Deserializer (SerDes) communications.

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