PREFACE

The Focus of This Book

Power integrity is a confusing topic in the electronics industry—partly because it is not well-defined and can encompass a wide range of problems, each with their own set of root causes and solutions. There is universal agreement that the field of power integrity includes everything from the voltage regulator module (VRM) to the on-die core power rails and on-die capacitance.

Between the VRM and die are interconnects on the package and board, which often carry discrete capacitors with their associated mounting inductance. The power distribution network (PDN) refers to all interconnects (usually inductive), the intentional energy storage devices (usually capacitive), and loss mechanisms (damping) between the VRM and the on-die Vdd-Vss power rails.

Power integrity is all about the quality of the power seen by the circuits on the die. What about noise created on the board power and ground planes by signals passing through cavities? Is this a signal integrity problem or a power integrity problem? Is the voltage noise generated by I/O switching currents and seen by the on-die Vcc and Vss rails a power integrity or signal integrity problem? Current that comes in through the common package lead inductance, which is ultimately connected to the VRM, generates this noise, which is sometimes referred to as switching noise or ground bounce.

This gray area between signal and power integrity has a profound impact on solutions that are offered for "power integrity" problems. Adding decoupling capacitors on the board often provide a solution for reducing Vdd core noise but seldom improve the cavity noise induced by high bandwidth signals. In general,

board-level capacitors offer little or no improvement to return-plane bounce noise. In some cases, the parallel resonances they create can actually increase the cavity-to-signal cross talk.

The first step to solving a problem is to clearly identify the problem and then correctly identify its root cause. A well-defined problem is often only a few steps away from a solution. Efficient solutions to problems are developed based on the actual root cause.

This book focuses on the specific power integrity problems related to noise on the Vdd rail, which powers the on-die core logic and enables it to perform functions. The gates powered by the on-die Vdd rail switch signals that communicate to other gates on the same die, and do not necessarily travel off die as I/O. Transient current caused by core activity causes noise on the Vdd rail, which is sometimes referred to as "self-aggression." The principles, analysis methods, and recommended best design practices to minimize this problem can also apply to other signal integrity, power integrity, and EMI problems; however, the focus in this book is on self-aggression of the Vdd rail.

Other Power Integrity or Signal Integrity Problems and Solutions

The term "power integrity" paints with too broad a brush to address all problems with general design recommendations. Instead, we need clear identification of the specific problem we are trying to solve, along with best design practices for each specific problem.

Some peripheral problems in a complete system design are sometimes categorized as power integrity:

- Noise on the Vcc-Vss rails from I/O switching, ground bounce, and switching noise: self-aggression by the Vcc rails
- Noise on the VRM output from its changing load impedance: self-aggression by the VRM
- Signal distortion as it travels through return path discontinuities: self-aggression by signals paths
- Noise from the power rails and VRM transferring onto and polluting the board-level PDN interconnects
- Cross talk between the voltage noise on the package and board-level PDN interconnects from all sources, coupling onto a Vdd rail
- Cross talk between the voltage noise on the package and board-level PDN interconnects from all sources, coupling to an I/O power rail

- Cross talk between the voltage noise on the package and board-level PDN interconnects and a signal which couples to the PDN

Each of these problems has a very different root cause and a different set of best design practices to reduce their impact. These topics are sometimes lumped under the signal integrity umbrella and sometimes the power integrity umbrella.

To avoid the possible confusion of assuming all power integrity problems are the same—and hence one set of solutions apply to all problems—engineers and designers should get in the habit of carefully articulating which problem is being addressed rather than using the general heading of power integrity or signal integrity.

A wealth of PDN design recommendations are offered in publications, at conferences, or by your favorite uncle. Blindly following any of them is dangerous. Unfortunately, many recommendations are either wrong or contradictory. This is partly because they are oriented toward only one of the specific problems listed above, but incorrectly generalized as the cure for all power integrity problems.

Be specific about the problem, the root cause, and the recommended best design practices.

Meeting the Challenge of Robust PDN Design

A poorly designed PDN can result in the product failing, usually at the worst possible time. PDN failures are difficult to diagnose because they are hard to reproduce. Sometimes they result from a very specific combination of microcode running a specific set of problems. This makes it difficult to "test in the quality" of a PDN. A robust PDN must be designed in.

Some PDNs may actually be robust with no additional considerations on the board other than a low impedance VRM. Other PDNs may require very specific combinations of capacitor values mounted in very specific positions, and then only run restricted microcode to be robust.

Every PDN is unique and has its own story. Each has its own combination of performance requirements, chip features, microcode, and design constraints on cost, performance, risk, and schedule. This makes it difficult to efficiently design a robust PDN by just following someone else's best design principles. That's where a solid design methodology plays an important role.

A common answer to many questions in any engineering field, including power integrity, is "…it depends." The only way to answer "…it depends" questions is by clearly defining the problem and then putting in the numbers and performing analysis of the specific problem, the root cause, and the various solution options.

The most efficient design process for the PDN (and most aspects of high-performance product design) so that there is a high probability of "getting it right the first time" is based on four elements:

- Start with the established best design practices.
- Understand the essential principles of how signals interact with interconnects—basically the principles of applied Maxwell's Equations.
- Identify the common problems to avoid and their root causes.
- Leverage analysis tools to efficiently explore design space and find the appropriate cost-performance-risk-schedule tradeoffs for each specific product's details and constraints.

The goal for many projects is to find an acceptable design that meets the performance objectives at acceptable cost, risk, and schedule.

This book is designed to be a handbook for the practicing power integrity engineer to establish a firm foundation in the principles of power integrity, identify the root cause of the common problems found in PDN design, follow the best design practices, and perform engineering trade-off analysis to balance cost, performance, schedule, and risk.

Who This Book Is Really For

As with all books in the Prentice Hall "Simplified" series, *Principles of Power Integrity for PDN Design—Simplified* minimizes the mathematical formalism to reveal the important engineering principles behind power integrity. If you are looking for detailed mathematical derivations and complicated numerical simulations, look elsewhere.

This is not to say that mathematical rigor is not important—every student of electrical engineering should have studied this in college. As a practicing engineer, being able to apply these principles to solve real problems is often more important than deriving every detail from Maxwell's Equations.

This book is based on a specific design methodology for high-performance systems. The starting place is to use established best design principles.

Unfortunately, every design is custom, they each have their own story. They each have their own set of performance goals and cost, risk, and schedule constraints. This means you cannot blindly follow every design guideline, but must use your engineering judgement.

This does not mean grab your 3D full-wave simulator and simulate everything. This would be an incredibly inefficient process with no guarantee of successfully converging on an acceptable solution.

The basis of engineering judgement is understanding the essential principles—which are really applied Maxwell's Equations—identifying the problems to avoid and their root cause, and leveraging analysis tools to efficiently explore design space to find an acceptable answer. This book is a guideline for applying this methodology to designing robust PDN systems.

As two experts in the signal and power integrity fields, with more than 70 years of engineering experience between us, we have distilled into this book what we consider to be the most important engineering principles upon which power integrity engineering is based.

Our experience is based on having personally worked on many designs, helping many engineers, and having to rescue many failed designs. We've seen the consequence of carrying around misconceptions based on a recommendation from the person you sat next to on your last airplane flight who has a nephew who once built a board that worked so must have done it correctly.

Engineers involved in the design process must become their own expert and not rely on what the last expert they talked to said about a product that has nothing to do with the one they are currently working on.

Enough mathematics is included to accelerate a practicing engineer up the learning curve to immediately perform trade-off analysis and identify what is important—and equally of value—what is not important.

Equations are used as a shorthand to clarify which terms are important and how they combine to influence the result. They are used to restate the principle with more detail. They are the first line of attack when "putting in the numbers."

Where possible, we show examples of simple simulations to illustrate the analytical approximations. Where appropriate, measurements from test vehicles and real systems are introduced to provide an anchor to reality that these principles actually work, as long as they are applied with good engineering judgement.

If PDN design is in your future, you'll find this book essential to your success.

Five Features That Make This Book Easy to Navigate

To engineer a more efficient process for using this book, we've incorporated five valuable features.

As with all books in the Prentice Hall Simplified series, we've tried hard to take the complexity of real-world problems and break them down to their simplest form to identify the essential principles and how they apply. Approximations are included as a way of quantifying the principles and applying them to specific problem examples. They are a first step to help calibrate our engineering judgement so we can make sense of simulation results.

Where possible, the results of an analysis are shown graphically in figures. The figures with their extended captions tell a story in parallel with the text and equations.

In each section, we've pulled out what we consider to be some of the most important conclusions or observations as TIPS. These reinforce the section's essences and make it easy when skimming the book to pick up or recall the highlights.

At the end of each chapter we've added "The Bottom Line" as a quick 10-point summary of the chapter's most important points. After reading the chapter, the 10 points should be obvious and expected.

Finally, the PDN resonance calculator spreadsheet used extensively in the last chapter is available on the book's companion web site at informit.com/title/9780132735551 and on the www.beTheSignal.com web site. Additional supplemental information on power integrity is available on these two web resource sites.

Outline for This Book

Principles of Power Integrity for PDN Design—Simplified is organized as a training manual for the power integrity engineer to learn the strategies, tactics, essential principles, and skills for successful PDN design.

Chapter 1, "Engineering the Power Delivery Network," provides a brief perspective on what the PDN is and why engineering a low impedance is so important. We introduce the idea of the impedance profile as an important design feature and indicator of PDN performance. We also introduce the most important figure of merit to describe the PDN design goal—the target impedance. Our goal is to engineer a PDN impedance profile below the target impedance with acceptable cost, risk, and meet performance and schedule targets.

Chapter 2, "Essential Principles of Impedance for PDN Design," provides a thorough review of impedance, which is the fundamental basis of evaluating a robust PDN. In particular, the properties of series and parallel RLC circuits are reviewed. These circuits determine the fundamental features of the PDN impedance profile. Simulation of the impedance profile of a collection of components is introduced as an essential skill. We show how any free version of a SPICE simulator can be used as an impedance analyzer.

Chapter 3, "Measuring Low Impedance," introduces measurement techniques for low impedance. Typical PDN target impedances range from 1 Ω to lower than 1 mΩ. Special techniques are used to measure the very low impedance of components and the entire PDN ecology.

Chapter 4, "Inductance and PDN Design," covers the essence of inductance, what it is, how it is affected by physical design, and how to estimate the loop inductance from physical design features. Engineering low loop inductance in the PDN interconnects is an important way to reduce peak impedances. When inductance cannot be eliminated, it is important to know how much there is so that its impact can be evaluated.

Chapter 5, "Practical Multi-Layer Ceramic Chip Capacitor Integration," reviews the properties of capacitors and how they behave individually and together. They are the primary component used to sculpt the impedance profile and manage the peaks. The five general tactics to reducing peak impedances from combinations of capacitors are introduced. In particular, the critical step of engineering low mounting inductance is introduced.

Chapter 6, "Properties of Planes and Capacitors," introduces the properties of critically important power and ground planes in the PDN interconnect, and how the capacitors interact with the planes. The most important property of the planes—the spreading inductance—is explored in detail. In addition, we show that the plane cavity resonances are not important at all for the quality of power seen by die circuits.

Chapter 7, "Taming Signal Integrity Problems When Signals Change Return Planes," explores another function of PDN interconnects: to provide a low impedance for the signal return currents. Switching noise, a form of ground bounce, is a problem that results in noise on the planes when signals pass through them. This is the realm of signal integrity and is separate and distinct from power integrity. Because the root cause of switching noise is different from PDN noise on the core Vdd rails, the solutions are very different. We are careful to distinguish this important signal integrity problem from power integrity.

Chapter 8, "The PDN Ecology," addresses the most important PDN feature: the peak impedance created by the on-die capacitance and the package lead inductance, and what can be done at the board level to reduce this peak. We show how to leverage all the design principles introduced up to this point to overcome the limitations created by this peak.

Chapter 9, "Transient Currents and PDN Voltage Noise," describes the features of the current drawn by CMOS circuitry, and how this current spectrum interacts with the PDN impedance profile. Three important transient current waveforms are introduced: a clock-edge impulse, a step transient current, and a repetitive square wave of current. These waveforms interact with different PDN features. Most importantly, we show how the three elements—impedance profile, transient current, and stimulated voltages—all interact. Knowing any two elements enables us to evaluate the third.

Chapter 10, "Putting It All Together: A Practical Approach to PDN Design," brings together all the principles and processes to illustrate how to design the specific features in the PDN to meet the performance goals. In particular, a simple spreadsheet–based analysis technique is introduced, which dramatically speeds up the process of creating a first-pass design. We walk through a few design scenarios and show an example of the power of the principles introduced in this book. From measured data, PDN parameters are developed that match measured performance incredibly well.

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