Practical Modeling of High-speed Channels Based on Data Sheet Input

Bert Simonovich
Lamsim Enterprises Inc.
lsimonovich@lamsimenterprises.com
As Dave Dunham from Molex Corp. likes to say, "When designing high-speed serial links beyond 10 GB/s, everything matters."
And part of that everything is accurate modeling of transmission line losses. It is important to model dielectric and conductor loss accurately. In this plot we see an example of a simulated transmission line with and without conductor roughness. Starting at the top, the red curve is the conductor loss without roughness. The next one down in blue is the dielectric loss. The pink curve is the sum of the dielectric and conductor loss without roughness, and finally the last curve in green is the total loss with conductor roughness.

\[ IL_{\text{total}}(f) = IL_{\text{dielectric}}(f) + K_{SR}(f) \times IL_{\text{conductor}}(f) \]
Failure to account for conductor roughness can ruin your day especially if you are trying to push 25 GB/s NRZ signaling down your channel. As shown with just 3.2 dB delta in insertion loss, at 12.5 GHz Nyquist frequency, results in ½ the eye height when conductor roughness is taken into account.
On top of that, failure to correct $D_k$ from data sheet due to conductor roughness can lead to inaccuracy in simulated insertion loss (IL) & phase delay.

Failure to correct $D_k$ from data sheet due to conductor roughness $\Rightarrow$ inaccuracy in simulated IL & Phase Delay
EDA Tool Challenges

Many EDA tools include latest and greatest models for conductor surface roughness and wideband dielectric properties. But obtaining the right parameters to feed models is always a challenge.

Many electronic design automation (EDA) tools include the latest and greatest models for conductor surface roughness and wide-band dielectric properties. But obtaining the right parameters to feed the models is always a challenge.

So how do we get these parameters?
One way is to follow the design feedback method which involves designing, building and measuring a test coupon. After modeling and tuning various parameters to best fit measured data, \( D_k \), \( D_f \) and roughness parameters can be extracted. They are then used in channel modeling software to design the final product.
But, as my friend Eric Bogatin often likes to say, “Sometimes an OK answer NOW! is better than a good answer late....” – Eric Bogatin

But, as my friend Eric Bogatin often likes to say, “Sometimes an OK answer NOW! is better than a good answer late.” As a high-speed signal integrity practitioner and backplane architect, I often have to come up with an answer sooner, rather than later because of the impact to time and cost to my clients. And that’s why I have been motivated over the last few years to research and develop a simple methodology to accurately determine parameters to feed into modern EDA tools.
What You Will Learn

✓ How to use my Cannonball model to determine Huray roughness parameters from data sheet alone
✓ How to determine $D_{keff}$ due to roughness from data sheets alone
✓ How to apply these parameters in the latest version of Polar Si9000e Field Solver
✓ How to pull it all together using Keysight ADS software
Outline

- Modeling Conductor Roughness:
  - Overview
  - Hammerstad Model
  - Huray Model
  - Cannonball-Huray Model
- $D_{keff}$ Due to Roughness Model
- Model Validation: CMP28 Platform / Polar Instruments Si9000e
- Example of Best Practice to Model High-speed Channels Based on Data Sheet Input: Amphenol-FCI ExaMax Backplane Reference Platform
Modeling Conductor Roughness
There are basically two kinds of copper foils used in the PCB world. They are rolled and electro-deposited copper foils. Rolled copper will always be smoother than ED copper, but is higher cost. ED copper is rougher and is most popular because of the lower cost.

It is important to note that ED copper has two sides to the foil. The matte side is the side facing the Cu sulphate solution. The drum side is the side facing the drum. The matte side is always rougher than the drum side.
Here are three common foil roughnesses used in the PCB industry today. The most common is standard profile on the left. It has no min or maximum IPC roughness spec.

Very low profile roughness, in the center, is typically any foil with a roughness of less than 5.2 microns.

Ultra Low profile copper, on the right, is a newer class of copper with roughness less than 2 microns max. There is no official IPC spec as yet, so you will see proprietary names like HVLP, ULP, VSP.
Foil nodulation treatment is applied to either the matte side or drum side of the foil. On the left are SEM pictures of the untreated drum and matte sides as they come off the electrodeposited process.

After going through the nodulation treatment, tiny nodules are deposited on one side of the foil as shown by the SEM photos on the right. Normally nodules are applied to the matte side, but it is becoming more common for nodule treatment on the drum side. This is referred to as reverse-treated foil or RTF. Double side treated foil is available but is not that common.
Typical tooth profile parameters reported in data sheets. The 10-point mean parameter ($R_z$), is the most common for the matte and drum side. It is the sum of the average of the five highest peaks and the five lowest valleys of the rough conductor surface over the sample length.

Sometimes average roughness ($Ra$) is reported for the drum side. And RMS roughness ($Rq$) may or may not be reported.
Here we see an example of how standard treated foil and reverse treated foil is bonded to core. The standard treated foil example sees the treated matte side bonded to the core, while reverse treated foil sees the treated drum side bonded to the core.

The important take away is that the nodule treated side is the one always bonded to the core laminate material, and is important to keep that in mind when you are modeling the channel.
The Hammerstad model has been used for decades to model conductor roughness, since all that was required was the RMS value of the peak to valley roughness parameter from data sheets. But it loses accuracy after 3-15 GHz, depending on the roughness of copper foil.
The Huray model has gained popularity over the last few years. It is based on non-uniform distribution of spheres resembling “snowballs” applied to a matte base. Although it is quite accurate, it is always difficult to obtain the right parameters for number of spheres, sphere radius and tile base area.

\[ K_{SBH}(f) = \frac{P_{\text{rough}}}{P_{\text{flat}}} \approx \frac{A_{\text{mate}}}{A_{\text{flat}}} + \frac{3}{2} \sum_{i=1}^{\infty} \left( \frac{N_i \times 4 \pi a_i^2}{A_{\text{flat}}} \right) \left( 1 + \frac{\delta(f)}{a_i} + \frac{\delta^2(f)}{2a_i^2} \right)^{-1} \]
It is theoretically possible to build an accurate snowball model of the surface roughness by extracting parameters through detailed analysis of SEM photographs. But practically, it is beyond the capabilities of most companies who do not have access to such equipment. Even if such equipment was available, the size, number of spheres and general tooth shape must be approximated anyways.

Early versions of the snowball model attempted to replicate real world roughness profiles by building facsimiles of low and high profile tooth structures, using a stack of uniform spheres, as shown. Each sphere had a radius of less than 1μm to fit a stack height of less than 5.8 μm RMS because that was the dominant size of snowballs, as measured from SEM data.

In this example, a hexagonal tile base, with a width of 9.4 μm RMS, was chosen to allow for replication into a lattice structure. Eleven spheres was the minimum number to fit within the hexagonal area and pyramid height of 5.8 μm RMS. Thirty-eight was the maximum number. By adjusting the number of spheres in this range shows excellent correlation to measurements.
Cannonball-Huray Model
This leads into what I like to call my Cannonball-Huray model. Using the concept of cubic close-packing of equal spheres, the spheres radius and tile area parameters for the original Huray model can now be easily estimated solely by the roughness parameters published in manufacturers’ data sheets.

This model can be used to optimally represent the surface roughness. As illustrated on the left there are three rows of spheres stacked on a square tile base. Nine spheres are on the first row, four spheres in the middle row, and one sphere on top. The height of the Cannonball stack is equal to the 10-point mean roughness $R_Z$ as published in foil manufacturer’s datasheets.

If we can peer into the stack, and visualize a pyramid lattice structure connecting to all the centers of the spheres, then the total height of the Cannonball stack is equal to the height of two pyramids plus two radii. Through simple geometry and a little bit of algebra we can approximate the radius of a single sphere $r = R_Z/16.73$ and base area, $A_{flat} = (6r)^2$:

Because the model assumes the ratio of $A_{matte}/A_{flat} = 1$, and there are only 14 spheres, the Cannonball-Huray model can therefore be simplified by the equation as shown on the right: Where: $K_{SR}(f)$ = roughness correction factor, as a function of frequency; $\delta(f)$ = skin-depth, as a function of frequency in meters; $r$ = the radius of spheres in meters; $A_{flat}$ = base area in sq. meters.
Modeling $D_{keff}$ Due to Surface Roughness
Everyone involved in the design and manufacture of printed circuit boards (PCBs) knows one of the most important properties of the dielectric material is $D_k$. When you compare simulation against measurements, you will often see a discrepancy in $D_{keff}$ due to increased phase delay caused by surface roughness.

In this case it is 3.6%
$D_{keff}$ is highly dependent on the test apparatus and conditions of how it is measured. There are several methods used in the industry. One method, commonly used by many laminate suppliers, is a clamped stripline resonator test method, described by IPC-TM-650 Test Method.

IPC-TM-650, section 2.5.5.5, Rev C, defines test methods to rapidly test dielectric material for permittivity and loss tangent, over an X-band frequency range of 8-12.4 GHz, in a production environment. The measurements are made under stripline conditions using a carefully designed resonant element pattern card, made out of the same dielectric material to be tested. The card is sandwiched between two sheets of unclad dielectric material under test. The whole structure is then clamped between two large plates, lined with copper foils that are grounded. They act as reference planes for the stripline.

By measuring a resonant frequency of the cavity, the effective permittivity and loss tangent are determined. The value of this method is to assure consistency of product, when used in fabricated boards. It does not guarantee the values directly correspond to design applications.
Therefore, Published $D_k$ not same as $D_{keff}$ due to roughness. This is a key point to keep in mind, and here is why.

Since the resonant element pattern card and material under test are not physically bonded together, as would be the case in real life, there are small air gaps between the various layers that affect measured results. These air gaps are caused, in part, by:

- Etching away the copper on material under test, leaving the bare substrate complete with the micro void imprint of the copper roughness
- The air gap between resonant element pattern card and material under test due to the copper thickness of the etch pattern
- The roughness profile of the copper, on the resonant element pattern card and fixture’s grounded foil reference planes, are different than would likely be in practice.
The illustration on the left shows an example of calculating capacitance between two smooth copper foil sheets bonded to each side of a dielectric material using dielectric thickness and $D_{keff}$ from data sheets. The separation is denoted by $H_{smooth}$ and is equal to thickness $t_{dielectric}$. If we know the cross-sectional area, $D_{keff}$ and thickness, capacitance $C_{smooth}$ is easily calculated.

The reality is that when copper with roughness is actually bonded to the core, under heat and pressure, we see the rough copper tooth profile being pressed into the prepreg as shown in the middle illustration. The effective separation between copper sheets is less, compared to smooth copper model. If we assume the separation between the plates is reduced to $(H_{smooth} - 2R_z)$, then the capacitance due to roughness $C_{rough}$ can be easily calculated by the middle equation shown.

Using $D_{keff}$ with rough copper model in the middle, is equivalent to using $D_{keff,rough}$ with smooth copper model, as shown on the right. If we do a little bit of algebra, we eventually come up with the simple equation, filled in yellow box, for $D_{keff,rough}$. This would then be used for impedance calculation and numerical simulations based on surface roughness, instead of effective $D_k$ value published in manufacturers’ data sheets.
For an FR408HR board with reverse treated foil, using data sheet values for $D_k$, we see that there is a difference of almost 4% between simulated and measured effective $D_k$ at 10GHz. But when we correct the $D_k$ due to roughness, we can improve the accuracy to within about 1%.
Model Validation
The CMP-28 Channel Modeling Platform from Wild River Technologies was used for model validation. It is an excellent platform for model development and analysis. It contains a total of 27 microstrip and stripline interconnect structures. All are equipped with 2.92mm connectors to facilitate accurate measurements with a vector network analyzer (VNA).
A VNA was used to measure a 2 inch, 2X thru, and an 8 inch long structure. The 2X through structure was then de-embedded using Simbeor software. A 6 inch GMS touchstone file was generated and used for later comparison.
The data sheet and PCB design parameters are summarized in the Table. Respective $D_k$, $D_f$, core, prepreg and trace thickness were obtained from data sheets.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>FR408HR/RTF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_k$ Core/Prepreg @ $f_s$</td>
<td>3.65/3.59 @10GHz</td>
</tr>
<tr>
<td>$D_f$ Core/Prepreg @ $f_s$</td>
<td>0.0094/0.0095 @ 10GHz</td>
</tr>
<tr>
<td>$R_s$ Drum side</td>
<td>3.048 μm</td>
</tr>
<tr>
<td>$R_s$ Before Micro-etch-Matte side</td>
<td>5.715 μm</td>
</tr>
<tr>
<td>$R_s$ After 50 μin (1.27 μm) Micro-etch</td>
<td></td>
</tr>
<tr>
<td>treatment-Matte side</td>
<td>4.445 μm</td>
</tr>
<tr>
<td>Trace Thickness, $t$</td>
<td>1.25 mils (31.73 μm)</td>
</tr>
<tr>
<td>Trace Etch Factor</td>
<td>60 deg taper</td>
</tr>
<tr>
<td>Trace Width, $w$</td>
<td>11 mils (279.20 μm)</td>
</tr>
<tr>
<td>Core thickness, $H_1$</td>
<td>12 mils (304.60 μm)</td>
</tr>
<tr>
<td>Prepreg thickness, $H_2$</td>
<td>10.6 mils (269.00 μm)</td>
</tr>
<tr>
<td>De-embedded trace length</td>
<td>6.00 in (15.24 cm)</td>
</tr>
</tbody>
</table>
Here we see SEM photos of typical surfaces for MLS RT foil. The left and center photos are the treated drum side and untreated matte side respectively. The right photo is a 5000x SEM photo of the matte side after etch treatment showing micro-voids.

An oxide or micro-etch treatment is usually applied to the copper surfaces prior to final lamination. This provides enhanced adhesion to the prepreg material. Typically 50 μin (1.27 μm) of copper is removed when the treatment is completed, depending on the board shop’s process control. The etch treatment creates a surface full of micro-voids which follows the underlying rough profile and allows the resin to squish in and fill the voids providing a good anchor.

Because some of the copper is typically removed during the micro-etch treatment, the published roughness parameter of the matte side is reduced by nominal 50 μin (1.27 μm) for a new thickness of 175 μin (4.445 μm).
The first step is to determine the effective $Dk$ due to roughness for core and pre-preg.

\[
D_{keff\_prepreg} = \frac{H_{smooth}}{\left(\frac{H_{smooth}}{2R_{z\_matte}}\right)} \times D_k\_prepreg = \frac{269 \mu m}{(269 \mu m - 2 \times 4.445 \mu m)} \times 3.59 = 3.713
\]

\[
D_{keff\_core} = \frac{H_{smooth}}{\left(\frac{H_{smooth}}{2R_{z\_drum}}\right)} \times D_k\_core = \frac{304.6 \mu m}{(304.6 \mu m - 2 \times 3.048 \mu m)} \times 3.65 = 3.725
\]
The next step is to determine the radius of spheres and base tile area for Huray model. Because electro-deposited (ED) foil has a matte side and drum side, with different roughness parameters, we must calculate the sphere radius for each side separately.

But most Huray models in EDA tools, including Polar Si900e, only allow one input for radius so I just take the average of the two for an effective radius ($r_{eff}$). Once we have that then it is easy to get the area ($A_{flat}$) of the flat tile base.
Here we see an example of Polar Si900e software main window and associated pop-up panels.

The first step is to select the “Lossless Calculation” tab at the bottom of the Si9000e main input window. When the pop-up window appears, choose the appropriate transmission line geometry from the pallet along the left-hand side, and then enter the specific design parameters in the boxes.

The next step is to select the “Frequency Dependent Calculation” tab at the bottom of the input panel and enter line length, conductivity and frequencies in the appropriate boxes in the main window.

Under the “Extended Substrate Data” section, choose “Causally Extrapolate Er / TanD” radio button and click “Edit” to enter the $D_{keff}$ parameters in a pop-up window as shown. Click “Calculate” to view causal $D_{keff}$ over frequency. Click “Close” to return to main window.

Under the “Surface Roughness Compensation” section from the main window, select Huray radio button and click “Edit” to enter the appropriate roughness parameters in the pop-up window. Enter $r_{eff}$ and $A_{flat}$ in the boxes shown. Enter 1.00 for “Ratio of Areas” and 14 for the “Number of Balls in Area” boxes. Click “Apply” to return to main window.

In the main window, hit calculate. Once the simulation has run, then export the touchstone file under the “File” menu if you want to save the s-parameters.
Here is the results of the simulation. As you can see there is excellent correlation for insertion loss and especially phase.
Well...single-ended looks great......BUT how well does this method work to model a practical backplane channel with diff pairs?
To demonstrate modeling High-speed channels, I will use the Amphenol-FCI Examax demo platform. This is a platform I helped design back in 2013 to showcase the Examax connector performance at 28GB/s NRZ. The Design Intent was to demonstrate 28 GB/s NRZ performance.

The same artwork supports Meg 6 or N4000-13EPSI material. Nelco N4000-13EPSI with MW-G-VSP ½ oz. foil (VLP) was used for this case study. The daughter cards used 2.9 mm coax connectors.

Four cases of different overall lengths were studied as shown.
This is a summary of the topology model. Both daughter cards were identical.

Breaking out of the coaxial connectors are 0.4 inches of single-ended trace before changing into 5.6 inches of differential pair routing. The backplane had 4 separate channels routed with various lengths shown.

Examax s-parameter models were also included.
Data Sheet Parameters [9], [10]

Here are the data sheet parameters highlighted with actual cores/prepregs used from the fabricator’s stackup drawing.
This is a summary of the transmission line geometry and design parameters from data sheets.
The first step is to determine the effective $Dk$ due to roughness for core and pre-preg of daughter card and backplane.
Similar to previous CMP28 Single-ended example, we determine the sphere radius and base area as shown.
Here we enter the parameters for daughter card single-ended trace portion and save a touchstone file
Then we enter the parameters for daughter card diff pair portion and save a touchstone file
And finally we enter the parameters for backplane diff pairs. We do this for Case 1-4 and save a touchstone file for each.
Keysight ADS is used to model and simulate the entire backplane channel, as shown here. The two schematics use the S-parameter pallet to model and compare the channel in the frequency domain.

All the Polar generated s-parameter files are concatenated together, as shown, including the Examax connector s-parameter files. Via and co-ax connector models are not included, because I want that “OK answer NOW!” You can always model and add them later to get that “good answer late.” if need be.
And here are the results for Case 1. In the left is the differential insertion loss SDD21. On the right is the differential TDR plot TDD11.

Remarkably there is excellent correlation for insertion loss and impedance!
Here are the results for Case 2. Similarly there is excellent correlation for insertion loss and impedance!
ExaMax Backplane Case 3 Total Length = 32.22"

Here are the results for Case 3. Still there is excellent correlation for insertion loss and impedance.
Finally here are the results for Case 4. Although there is slightly more loss than measured, there is excellent correlation for insertion loss and impedance.
These two schematics use the “ChannelSim” pallet for transient simulation and eye diagram analysis.
This slide shows plots of transmit eyes on top and receive eyes on bottom at 28GB/s. The simulated channel is on the left and the measured channel is on the right. Even though the measured transmit eye on the top right shows slightly more noise and jitter, the received eyes are virtually the same.
Similarly the longest length with slightly worse simulated loss shows virtually no difference in received eye opening suggesting the “OK answer NOW!” is probably good enough to make an engineering decision.
Summary

By using Cannonball-Huray model, with copper foil roughness and dielectric material properties obtained solely from manufacturers’ data sheets, a practical method of modeling high-speed differential channels is now achievable using commercial field-solving software employing Huray model.
References:

3. B. Simonovich, “Practical Model of Conductor Surface Roughness Using Cubic Close-packing of Equal Spheres”, EDICon 2016, Boston, USA
6. Wild River Technology LLC 8311 SW Charlotte Drive Beaverton, OR 97007. URL: http://wildrivertechnology.com/home/
7. Simberian Inc., 3030 S Torrey Pines Dr. Las Vegas, NV 89146, USA
8. Isola Group S.a.r.l., 3100 West Ray Road, Suite 301, Chandler, AZ 85226. URL: http://www.isola-group.com/
16. ISOLA-Group, “Copper Foil 102 Presentation”, 2012
Thank You!

Lamsim Enterprises inc.
Innovative Signal Integrity & Backplane Solutions

Lamsimenterprises.com